

# Design and Verification of Car Parking Management System Using Verilog

Vamshi Achha<sup>1</sup>

<sup>1</sup> Department of Electronics and Communication Engineering,  
M-Tech, Vaagdevi College of Engineering, Warangal, India

Dr. M. Shahsidhar<sup>2</sup>

<sup>2</sup> Principal & Professor Vaagdevi Engineering College, Warangal, India

## Abstract

This paper presents the design and verification of a car parking management system using Verilog HDL. The system monitors vehicle entry and exit, tracks available parking slots, and prevents overflow conditions. The design is implemented using register transfer level (RTL) modeling and verified through simulation tools. The results demonstrate accurate slot tracking, proper full and empty detection, and reliable operation under different test scenarios. The proposed system offers a scalable and efficient solution for automated parking management.

## Keywords

Verilog, RTL Design, Finite State Machine(FSM),, Parking System, Digital System, Simulation, Digital System design

## 1. Introduction

With the rapid increase in the number of vehicles, efficient parking management systems have become essential. Traditional manual parking systems lead to congestion, human errors, and inefficient utilization of parking space. Automated parking systems improve accuracy, reduce manual effort, and enhance operational efficiency. FPGA-based systems provide high-speed processing and parallel operation advantages compared to microcontroller-based systems. This paper presents the design and simulation-based verification of a car parking management system using Verilog HDL.

## 2. Literature Survey

Several parking management systems have been implemented using microcontrollers, IoT platforms, and FPGA technologies. Microcontroller-based systems offer simplicity but have

limited parallel processing capability. IoT-based systems provide remote monitoring but introduce communication latency. FPGA-based systems.

### **3. Proposed System**

The proposed system consists of entry sensor, exit sensor, counter module, control logic, and display module. When a vehicle enters, the counter increments. When a vehicle exits, the counter decrements. If the parking slots reach maximum capacity, the system disables entry and indicates a parking full condition. If all slots are empty, it indicates parking empty. The system operates synchronously using clock and reset signals.

### **4. Design and Implementation**

The system is developed using Verilog HDL with RTL modeling style. The design includes synchronous up/down counter, finite state control logic, slot availability comparator, and output status indicators. Simulation and verification are performed using tools such as ModelSim or Xilinx Vivado. Different test cases validate normal entry, exit, full detection, empty detection, and reset behavior.

### **5. Results and Discussion**

Simulation results confirm correct increment and decrement functionality. The system accurately detects full and empty conditions without overflow or underflow errors. Waveform analysis shows stable signal transitions and proper synchronization with the clock signal. The modular structure allows scalability for larger parking capacities.

### **6. Conclusion**

The proposed car parking management system efficiently monitors parking slots using Verilog HDL. The RTL-based modular approach ensures scalability and reliability. Simulation results validate correct system functionality. The design can be implemented on FPGA hardware for real-time parking applications. Future work may include integration with IoT modules for remote monitoring.

### **References**

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