A pragmatic review of buck-boost converter optimization models from an empirical perspective

Chandini Mutta[1], Agam Das Goswami[2]
1,2 VIT-AP University, Amaravati, Andhra Pradesh- India.
Corresponding author: e-mail: agam.goswami@vitap.ac.in

Abstract: Buck-boost circuits assist in increasing or reducing input voltage levels to suit different load types. Optimization of these circuits enhances their DC-to-DC conversion efficiency in terms of output THD (Total Harmonic Distortion), conversion accuracy, reduction in inductor conduction losses, reduced power dissipation in the MOSFETs, lower power loss in the filter capacitor, and low diode conduction loss levels. A wide variety of machine learning-based models are proposed for the optimization of these converters, and each of them varies in terms of their internal characteristics, and external circuit dependencies. Moreover, most of these optimization models have different performance levels under different circuit conditions. Thus, it becomes difficult for circuit designers to select efficient optimization models for their functional and performance-specific use cases. To overcome these issues, this text initially discusses the design of various buck-boost converter topologies and their optimization techniques. These optimization techniques are studied in depth, which will assist readers to identify optimal techniques for their deployment-specific use cases. Based on this in-depth study, it was observed that deep learning models for component rating selection, optimization models for duty cycle selection, and machine learning-based models for load-based optimizations are highly recommended for real-time deployments. This text also compares the reviewed models in terms of their performance metrics including resultant THD levels, conversion efficiency, computational complexity, scalability, and conversion delays, which will allow readers to evaluate performance-specific models for their deployments. To further simplify the model selection process, this text proposes an evaluation of a converter optimization rank metric (CORM), which combines these performance metrics to identify models with higher conversion efficiency, lower THD & complexity, and faster response under real-time scenarios.

Keywords: Buck, Boost, Converter, THD, MOSFET, Optimization, Machine, Learning, Duty, Cycle

1. Introduction

Buck-boost converters are fundamental components in modern electronics, serving as versatile tools for transforming DC voltages to cater to varying load requirements. In scenarios where input and output voltage sources are incompatible, these converters bridge the gap, enabling seamless integration of different voltage levels. Their application spans across diverse domains, including portable devices, renewable energy systems, and power management solutions. However, the dynamic nature of these nonlinear systems presents challenges in achieving efficient DC-DC conversion.

Efforts to optimize buck-boost converter performance have gained paramount importance, driven by the pursuit of increased conversion efficiency, reduced power losses, and improved component selection. These optimization endeavours are crucial for meeting stringent

requirements such as minimizing Total Harmonic Distortion (THD), mitigating conduction and switching losses, and optimizing component ratings for optimal converter operations.

In this context, the present paper undertakes a rigorous exploration of various optimization models tailored to buck-boost converters. The central goal is to provide empirical insights and practical guidance for circuit designers facing the complex task of model selection. The paper dissects the internal characteristics and external dependencies of these models, highlighting their performance variations under different circuit conditions.

The subsequent sections delve into the myriad applications of buck-boost converters, elucidating their role in voltage transformation for electronic devices and their integration within hybrid energy systems. Different buck-boost converter topologies are examined, each catering to specific voltage transformation needs. By thoroughly evaluating the operational principles, benefits, and limitations of these models, readers are equipped to make informed decisions based on their unique deployment scenarios.

To simplify the model selection process and facilitate informed decisions, the paper introduces the Converter Optimization Rank Metric (CORM). This metric amalgamates performance indicators such as conversion efficiency, THD levels, computational complexity, scalability, and conversion delays. This holistic approach empowers circuit designers to identify models that offer superior conversion efficiency, lower THD, reduced complexity, and prompt responses in real-time applications.

In conclusion, the ensuing sections of the paper dissect various optimization models for buck-boost converters, enabling readers to assess their applicability and performance under diverse operational conditions. The proposed CORM framework adds an essential tool to the circuit designer's arsenal, aiding in the selection of optimal models for specific deployment scenarios.

Problem Definition

DC-DC converters are essential in the field of power electronics for changing the level of direct current voltages. The integration of numerous components inside electronic systems is made possible by this transformation, which is required to close the gap between incompatible input and output voltage sources. The buck-boost architecture among these converters occupies a prominent place since it can step up and step-down input voltages, making it adaptable for a variety of applications.

Buck-boost converters are important, but they are not without difficulties. The effectiveness of these converters is crucial, especially in the energy-conscious world of today. These systems' innate nonlinearity and dynamic nature add complexity and have an effect on how well they operate overall. The design and optimization process is further complicated by factors including Total Harmonic Distortion (THD), power losses, component conduction and switching losses, and voltage regulation accuracy.

Numerous optimization strategies and models have been developed in an effort to increase the effectiveness and dependability of buck-boost converters. By optimizing various parts of the converter's operation, these strategies seek to address the aforementioned difficulties. To obtain desired performance metrics while reducing losses and distortions, variables like duty cycle, component ratings, and control techniques must be tuned.

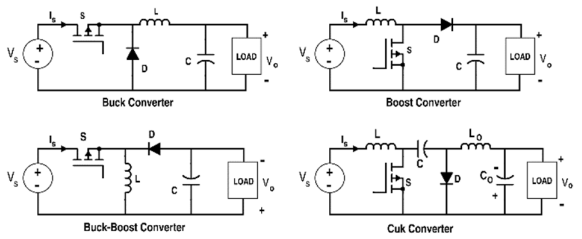

Figure 1. Different converter topologies

How can we systematically tune buck-boost converters as shown in Figure 1, to obtain increased efficiency, decreased power losses, and higher output quality is the main issue this proposed article aims to solve. The fact that many buck-boost converter models exhibit diverse characteristics and performance differences under various circuit settings further adds to the complexity of the issue. Real-world applications, where variables like load variations, input voltage fluctuations, and dynamic load demands are present, highlight how complex this situation is.

This issue has important practical implications. Consumer electronics, renewable energy systems, and hybrid energy architectures are just a few areas where effective buck-boost converters are used. The entire performance of the system in which a converter is incorporated may be constrained by a poor converter design's potential for reliability issues, higher power losses, and reduced efficiency levels. For engineers and designers, this makes choosing and implementing the appropriate optimization models extremely important for different use cases.

Therefore, the difficulty lies not only in understanding the nuances of the many optimization strategies suggested in the literature but also in deciding which model is best for a particular application case. Conversion efficiency, THD levels, computational complexity, scalability, response times, and adaptability to changing load conditions are just a few of the many variables that must be considered throughout this selection process. Additionally, because these components interact, the design process is a multidimensional optimization issue.

It gets even more complicated because optimization techniques can easily become obsolete or less efficient due to the dynamic nature of technology and changing applications. The goal of this work is to give practitioners the skills they need to critically analyze, compare, and choose optimization models that fit their particular application needs and environmental circumstances. As a result, it goes beyond simply giving an overview of current methodologies.

In conclusion, the key issue of the suggested study is the optimization of buck-boost converters for increased effectiveness, decreased losses, and higher output quality. This entails investigating the wide range of optimization models, comprehending their complexities, and developing a framework to methodically assess and choose the models that are best suited for deployment in the actual world. The goal of this article is to promote efficient and dependable power conversion technologies for use in a variety of sectors and applications.

2. Literature review

The efficiency of buck-boost converters has been improved by the introduction of numerous optimization models. However, depending on their internal workings, each model's efficacy differs. One study uses a generalized state-space average model (GSSAM) to examine multiphase interleaved buck, boost, and buck-boost converters [1]. GSSAM replicates the switching behavior of current and voltage waveforms, making it appropriate for multi-converter resonant high-current-ripple systems, whereas the average model just reflects average values. The three-phase buck, boost, and buck-boost

converters covered by this paper's extension of GSSAM are used to show the applicability of the model to different converter phases and its potential to replace several process steps. This is confirmed by contrasting the transient and steady-state dynamics of the GSSAM with those of the PLECS switching models.

System designers have created two-switch enhanced gain buck-boost converter (EGBBC) topologies for higher-voltage applications [2]. These topologies allow for a voltage shift from ground to buck to boost by reconfiguring ZETA cascaded boost and following cascade of boost. To solve this problem, the Type-1, Type-2, and Type-3 quadratic buck-boost voltage gain topologies are proposed by researchers at the Energy Frontier Research Center (EFRC). Through closed-loop system measurements, it is discovered that EGBBCs have advantages over traditional buck-boost converters in terms of stability, robustness, and voltage control.

[3] examines how well buck-buck/boost PFC converters work to minimize input current dead zones in buck PFC converters. Frequency-Offset Time-Ratio Control (FOTRC) and Frequency-Duty-Cycle Ratio Control (FDCRC) are recommended for CRM/DCM buck-buck/boost PFC converters to increase power factor (PF) at low input voltages. By switching to the advised controls, PF is improved by modifying the on-times or duty cycles of the buck/boost and buck modes over a wide input voltage range. Additionally, methods to improve dynamic response performance under load or input voltage fluctuations are provided, such as Smooth and Rapid Dynamic Response Control (SRDRC).

For grid systems, a single-inductor linear buck-boost switched-mode audio amplifier with this power architecture is presented [6]. When compared to two-step conversion, the amplifier uses single-step class-D (SSCD) conversion to increase power output to speakers while improving efficiency. By using a freewheeling inductor with a specified de-energizing phase for linear control transmission, efficiency is increased.

The unique input-parallel output-series buck-boost converter (IOBBC), with its high voltage gain, numerous output voltages, improved efficiency, and reduced output voltage and source current ripples, is introduced in [4, 5]. Two different buck-boost converter topologies are used by the IOBBC, both of which operate in parallel-series mode. The K-factor technique and particle swarm optimization make closed-loop control design possible.

The Interleaved Tri-state Buck-Boost converter (ITBBC) is advised for grid-based models [5]. ITBBC performs better than traditional Interleaved Buck-Boost converters (IBBC) by removing dead zones during mode transition. A Type-III controller upgrade enhances stability and transient responsiveness. Superior transient response, less ripples, and more effectiveness are all attributes of ITBBC.

Dual-mode operation of the H-bridge buck-boost converter is investigated [9], overcoming issues with voltage gain oscillation and dead zones during mode transitions. With the introduction of dead-zone free control (DZFC) technology, efficiency and dynamic performance, particularly in transition modes, were improved. DZFC offers a potential solution for quick payback or instant performance increase and improves transient responsiveness.

Additionally, buck-boost-buck resonant LED drivers are suggested [8], which adjust the power factor and current balance with a single switch. The LED driver uses storage and resonant capacitors to automatically balance the current

across outputs, improving efficiency and streamlining management.

For the noninverting buck-boost (NIBB) converter, an analog multiplier-based controller is suggested [8], allowing for smooth switching between the buck and boost modes. The CMOS-developed controller automatically modifies performance based on input and output voltages.

Variable speed drives (VSDs), which address the high energy use by electric motors, are crucial for energy efficiency. For three-phase buck-boost inverter systems, the return route inductor Y-inverter (RPI-YI) is a ground-breaking design [7]. RPI-YI dramatically lowers magnetic volume and current strains on inductors by transferring buck-boost inductors from forward current channels to the return route, making it a promising solution for modular buck-boost VSD devices & samples.

The work in [11] focuses on optimizing Type-III Compensators with the Dragonfly Algorithm (DA) for two-stage Interleaved Buck-Boost Converters (IBBCs) [10]. In a dual-phase inverting Buck-Boost converter (IBBC), two identical Buck-Boost converter (BBC) cells are connected in parallel with a 180-degree phase shift. In terms of dynamic performance, efficiency, source current ripple, and output voltage ripple metrics, the closed-loop IBBC with the DA-optimized Type-III controller beats both conventional Buck-Boost (BBC) converters and IBBCs outfitted with conventional Type-III controllers. The experimental and numerical validations of the suggested control approach are encouraging.

Environmental elements including temperature, shadow, and irradiance have a considerable impact on solar panel voltage in the context of high-voltage systems [12]. A buck-boost inverter is required to handle the wide range of DC voltage swings. For significant PV output voltage swings, this article introduces single-phase, single-stage buck-boost inverters using five switches. With voltage source inverters, PWM dead-time problems are resolved by these inverters. Leakage current is decreased and reactive power capabilities are increased by coupling the negative terminal of the PV panel to the grid's neutral. The paper presents a high-gain buck-boost inverter that makes use of a number of methods, such as quadratic boost and switching inductors, to obtain controlled duty ratios and generate boost voltage inversions. Lab prototype inverters are used to verify the theoretical ideas.

[13] proposes a bipolar buck-boost ac-ac converter (NBB IANM TCDR) with noninverting buck, boost, inverting, and configurable noninverting modes. The unidirectional buck circuits used by this converter increase reliability by allowing it to survive situations when there is an open circuit or a short circuit. By preventing the dead-time issues caused by pulse width modulation, the converter ensures safe commutation without the use of extra soft-commutation techniques. External rapid recovery diodes reduce power loss and high-frequency conduction, enhancing converter performance. This converter aids in the grid's ability to restore voltage dynamically.

Solar photovoltaic (PV) systems are becoming more popular as a result of growing fossil fuel prices and environmental concerns [14]. The study of a three-port DC buck-boost converter (HSUD TPCB) with two one-way and one two-way ports for solar energy to charge batteries. The suggested converter uses step-up/down and buck-boost converters to support bidirectional energy flow, increasing efficiency and smoothing out the power supply. Experimental tests are used to confirm theoretical predictions.

The article [15] describes a single magnetic core, bridgeless, single-phase buck-boost power factor correction (PFC) converter. The converter uses a discontinuous capacitor voltage mode with a low Total Harmonic Distortion (THD) for constant input current. Its effectiveness and ease of control are significant because it does away with the requirement for additional circuitry to lessen input current dead angle. Laboratory prototypes support theoretical findings, which are discussed along with the study's historical context and converter philosophy.

A buck/boost SIMO dc-dc converter with average current regulation is introduced in the post [16]. The inductor current reference stability and output channel cross-regulation are guaranteed by the new charge-balance system and auto-tuning duty generator. Cross-regulation during loading transients is further decreased by the anti-right-half-plane-zero method. The converter's efficiency and transient response have been verified in lab experiments.

There is a single-phase bipolar buck-boost direct ac-ac converter presented [17]. There are various ways that this converter can function, and it provides distinct voltage gains for both buck and boost operations. Reactive load input and output features of the converter allow for grid voltage stabilization as shown in figure 2 for ON & OFF States.

A simple bidirectional converter turn-on snubber is suggested by the designers [18]. This snubber considerably lowers the switching-off current loss in the converter's main diode, decreasing primary and reverse recovery losses. Laboratory tests confirm the performance improvement over conventional bidirectional converters.

For effective dc voltage use, flyback-type buck-boost inverters working in discontinuous conduction mode (DCM) are explored [19]. The study presents a pulse energy modulation (PEM)-based method for DCM/CCM conversion in single-phase buck-boost inverters. The PEM approach improves the efficiency of dc voltage consumption and has implications for simulations of single-phase buck-boost inverters.

The Manitoba Rectifier is a ground-current-operated bridgeless buck-boost power factor corrector [20], which is presented by electronic circuit designers. In this setup, an LC filter is used to deliver a constant grid current to a buck-boost circuit's input, substantially lowering ripple voltage. Laboratory prototypes attest to the design's usefulness.

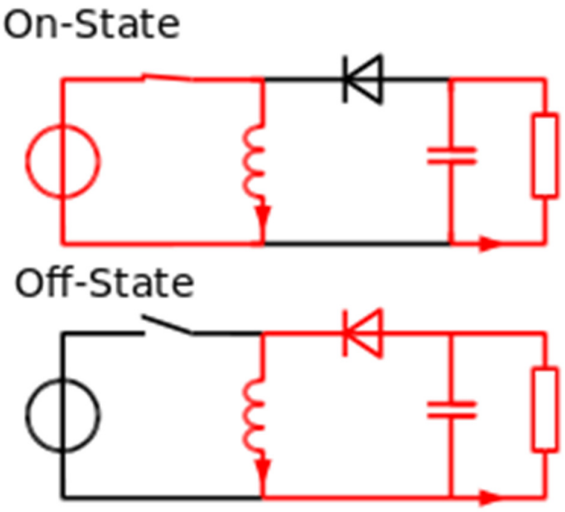

Figure 2. Operations in ON & OFF States

Maximizing power extraction from two serially linked subarrays utilizing a single-phase transformer-less grid-connected solar converter with coupled inductors (SCA CIBB) is the focus of the study presented in [21]. This converter connects two subarrays in series using a buck-boost inverter, substantially cutting the number of modules needed for each subarray in half. Even though the two subarrays are fundamentally different, they can each work independently to provide the most power. When compared to single-inductor buck-boost

approaches, the use of coupled inductors minimizes the complexity, size, weight, and footprint of the converter while providing improved overall efficiency at higher output powers. Regardless of the operation mode (CCM or DCM), a specific inductor current controller ensures grid current control while keeping a low leakage current from the subarray. Experimental testing with a 1 kW power output is used to verify the performance of the proposed converter.

Single-phase matrix converters (SPMCs), which are essential for dynamic voltage restorers and have step-changed frequency operation and bipolar voltage gain, are becoming more and more popular among high-voltage system designers [22]. Eight IGBTs, second-order input and output filters, a tiny film capacitor, and an effective single-phase buck-boost MC are used in this work. The 16 switches used in the cascaded buck-boost MC operation efficiently reduce component voltage/current strains and ripples. The paper introduces several modulation and buck-boost approaches. The converter improves performance under non-uniform power factor load conditions by maintaining constant currents at the input and output. A 400 VA prototype converter is used in laboratory testing to gauge the proposed converter's performance.

In [23], interleaved buck-boost converters are suggested as a way to simplify power electronics systems. An inverter (NPIB) is created by combining a buck converter with several parallel interleaved boost converters. The buck switch simply activates the boost switch, simplifying control and enabling soft start/stop functionality. When a load fails or is overloaded, the buck stage serves to cut off power to the electronics. The converter can also work as a high-voltage interleaved boost converter thanks to the similar switching method. The study provides in-depth analysis and graphical representations of required clearances for the non-overlapping gate signal sections of the three-phase interleaved buck-boost converter. The dc-dc or ac-dc converter's practical use is simple, and additional test scenarios are used to evaluate the converter's performance.

In [24], an adaptive window mode selection is investigated to improve the ripple regulation (AW MRR) of a non-inverting buck-boost dc-dc converter. The suggested mode selection makes it simple to switch between buck and boost modes, allowing the converter to operate in the mode that is most appropriate for the task at hand. Utilizing mixed-signal polypide technology with a 0.35 m CMOS 2P4M 3.3V/5V, the study achieves a maximum conversion efficiency of 97%.

[25] describes a buck-boost converter with phase interleaving. An interphase transformer (IPT) can increase power density, lower inductor ripple current, and double ripple frequency in a dual interleaved buck-boost converter. To attain high power density, the study develops a 32-kW dual interleaved SiC prototype with an IPT. The prototype has a high level of efficiency and can output 315 to 385 V.

For applications requiring unidirectional power transmission and a broad buck-boost voltage conversion range, the semi-dual-bridge resonant isolated dc-dc converter (SDBRC) family is investigated in [26]. The study discusses voltage conversion ratios, transfer power, and coordinated control methodologies while presenting a three-tiered SDBRC. By lessening voltage stress on power equipment, the suggested architecture attempts to cut costs and power losses. The study backs up its theoretical analysis with real-world evidence.

[27] examines two cutting-edge PFC rectifiers with voltage buck-boost characteristics. These rectifiers don't require antiparallel diodes and use

fewer semiconductors. When used in the discontinuous conduction mode, the rectifiers deliver nearly pure input currents that are unaffected by harmonics. Through extensive laboratory testing, the study confirms the validity of its theoretical findings.

Full-bridge single-stage transformer-free buck-boost inverters are frequently used by grid system designers [28]. These inverters offer single-stage input voltage stepping, reactive power control, continuous output current, user-specific actions, and continuous output current. The study introduces the H8 and H6 buck-boost inverters and uses rigorous testing to show how much more efficient they are than current ones.

The buck-boost voltage source inverter design and control technique (TL SS BB) introduced by the authors of [29] does not require a transformer. The inverter's structure, mode of operation, and modulation technique are described in detail in the paper, which supports its feasibility through theoretical analysis and actual testing.

A six-switch buck-boost Y-inverter (6YI) is investigated in [30] with the use of switching techniques such as discontinuous pulse width modulation (DPWM) and third harmonic injection pulse width modulation (TPWM). The study emphasizes how DPWM can reduce energy lost in conduction, resulting in a system that is more effective with peak efficiency at nominal loads. The theoretical conclusions are supported by a hardware prototype & process.

The use of buck-boost power conditioners to adjust the electrical voltage from renewable energy sources, which can change owing to weather conditions, is covered in the study mentioned in [31]. The single-inductor buck-boost inverter is the subject of study specifically. The inverter may function in both directions without high-frequency common mode (HFCM) voltage since the duty ratio affects the output voltage. The power density of the suggested inverter is greatly increased by adding a single inductor to the power train. The inverter is practical and effective since it uses only two switches that can handle high frequencies. A full-bridge inverter is used as the base for a cascaded buck-boost inverter. The benefits of the full-bridge inverter are still there in the cascade design. The performance of the recommended full-bridge inverter is experimentally verified after theoretical analysis, utilizing hardware prototypes. The article shows that the cascaded inverters achieve 220 V, 60 Hz, and 1000 W output whereas the full-bridge single-inductor-based buck-boost inverter achieves 110 V rms, 60 Hz, and 500 W output.

Automotive buck-boost converters should not be inverted for high-voltage applications, according to [32]. The converter in the study makes use of bootstrap capacitors, a novel controller chip, off-board NMOS power transistors, and NMOS power transistors. It investigates several operating modes, including as buck and boost modes, and applies current sensing to control. The suggested converter achieves efficiency up to 96.1% at a load current of 1.5 A and a switching frequency ranging from 600 kHz to 1 GHz. It supports a wide input voltage range (7 to 60 V) to accommodate battery voltages in cars.

[33] offers an ac-dc driver (AAD IBBC) with a buck and boost converter for offline LED drivers with great power density. High power factor (PF), low total harmonic distortion (THD), and high-power density (PD) are achieved by the converter. The suggested converter streamlines the design and improves power quality by integrating the buck and boost stages into a single component (FIBBC).The study establishes a new standard for converter efficiency by showing a 92.62% efficiency, 0.99

PF, 10% THD, and 6% ripple in the output current for the FIBBC.

Work in [34] offers transformer-free solutions for photovoltaic (PV) inverters employing dual-mode time-sharing (DMTS) for grid networks. The suggested converter achieves up to 97.6% efficiency in step-down or step-up conversion modes and less than 2% total harmonic distortion of the injected current. In order to accurately regulate the current, the study uses quick dead-beat control to address the issue of leaking current.

A high-frequency buck-boost ac-ac (SBT-HFI-BBAC) converter with symmetric bipolar isolation on a single phase is discussed in [35]. This converter includes a high-frequency transformer (HFT), input and output LC filters, two full-bridge inverter modules, and additional parts. It functions in both noninverting and inverting buck-boost modes, and the output voltages are similar thanks to the symmetric bipolar voltage gains. The study outlines possible uses for the converter in a variety of situations, such as improving power quality and restoring dynamic voltage.

In [36], researchers look into high-power output voltage oscillation and system instability in noninverting buck-boost converters' operational dead zone during mode changeover. In order to solve the dead zone issue, the study presents a multimode smooth switching control method, concentrating on boost and buck modes for enhanced stability and operational power.

Unique power inverter topologies are suggested in [37] in order to maximize power density, efficiency, and reliability. For a variety of applications, single-phase, single-stage buck-boost inverters with output unfolding circuits (SSB OUC) are investigated. These inverters can be integrated with renewable energy sources and energy storage systems because as per Figure 3, they are designed with PWM to feed reactive power back into the utility grids.

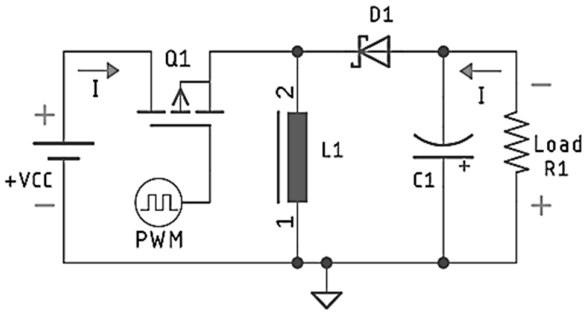

Figure 3. PWM Operation in the Converters

Work in [38] describes a triple-mode isolated resonant buck-boost converter (TMIR) for home fuel cells and solar panels. To handle a wide input voltage range, the converter operates in step-down, step-up, and pulse width modulation series-resonant buck modes. In comparison to conventional resonant converters, the suggested triple-mode converter is more effective and needs less specialized components.

A noninverting buck-boost DC-DC converter with magnetic coupling between the input and output states is the subject of research in [39]. To deal with the difficulties of operational dead zones and phase behavior during mode changeover, they use direct model predictive control (DMPC). By reducing the amount of time that passes between switch activations, DMPC improves control performance.

A trustworthy family of ZETA converter topologies is used to propose a transformer-free buck-boost converter in the paper discussed in [40]. With this converter, buck-boost functionality, dc isolation, and constant output current are all achieved. The suggested converter uses less power and is more efficient because it has a larger voltage gain than conventional ZETA converters.

The benefits of a two-stage cascade architecture for modular power supplies are covered in [41]. Power switches are used in this architecture to minimize the overall amount of components required for a cascade system. The integration of an LLC resonant converter (LLC RC FSN) and a noninverting buck-boost converter with four switches is suggested in the study. By canceling out currents from the buck-boost stage and the LLC stage during idle times, this method improves efficiency and lowers conduction loss. An experimental 720-W prototype with a maximum efficiency of 96.4%, an input voltage range of 250 to 440 V, and a promising transformation performance is produced.

A three-phase interleaved buck-boost-derived power factor correction (PFC) converter for more electric aircraft (MEA) is shown in [42]. By achieving unity power factor at MEA's broad supply frequency, this converter hopes to increase power density, consistency, and efficiency. The advantages of the suggested converter are shown by contrasting it with a single-cell, three-phase buck-boost-derived PFC converter. The prototype circuitry achieves an input current total harmonic distortion (THD) of 2.52% and a power factor of 0.9996.

Modular energy storage systems typically call for intricate equalizers and central converters. Work in [43] investigates the usage of half-bridge cell equalizers (HBCE) in cascaded buck-boost converters for energy storage modules. By utilizing half-bridge cells within each module, these equalizers reduce the need for equalizers at the module level and preserve voltage parity between modules. A prototype shows how the converter can transfer electricity in both directions while keeping the voltage constant between cells and modules.

Work in [44] focuses on gate drivers for high-voltage buck and boost converters that use GaN-based half-bridge structures (GAN HBS). The gate drivers use a three-level architecture to reduce problems with pulses brought on by quick voltage changes. Dead time management improves performance under light loads, resulting in gains in buck and boost converter efficiency of 8.33% and 6.88%, respectively.

Work in [45] advocates employing power MOSFETs to increase the efficiency of dual-buck dc-ac inverters and dual-boost ac-dc converters. Large magnetic volume and several inductors-related problems are addressed by the design. By utilizing fewer inductors, the suggested designs, known as dual-buck inverters (DBIs) and dual-boost converters (DBCs), minimize the magnetic mass, expense, and complexity. A prototype 2-kW cascaded dual-buck dc-ac inverter converts 310 V dc input voltage to 440 Vrms output voltage efficiently for different use cases.

Work in [46] explores the use of multilayer inverters with built-in voltage-boosting capabilities. In a five-stage asymmetric architecture, the study uses PPBB DC/DC converters and suggests a particular configuration for the primary DC/DC converter. A 1.5 kVa laboratory prototype of the proposed converter showed enhanced power density, efficiency, and modulation characteristics, reaching a peak efficiency of 98.7%.

[47] offers a control mechanism that uses a second-order switching surface with Buck-Boost Converters (BC) to improve the responsiveness and dependability of switching power converters. Conduction and switching losses are reduced by the control system, increasing conversion efficiency.

[48] uses the delta-sigma modulation (DSM) approach to regulate the power switches in a buck-boost inverter. The converter's operating mode is dynamically chosen by the DSM

controller, allowing for easy switching between modes. The method's efficacy is demonstrated through a CMOS-based prototype.

A control method for buck-boost inverters in photovoltaic (PV) systems is presented in [49]. The control system guarantees the AC power grid's dependability and homogeneity of power transformation.

The application of adaptive sliding-mode control for a high-efficiency buck-boost converter built on a Zeta architecture is covered last in [50]. Compared to conventional Zeta converters, the controller improves efficiency by adjusting the inductor's proportional term and erroneous current levels. There is no doubt that bio-inspired and deep learning models perform better than their counterparts. In the following section of the article, we will compare and contrast several methods with respect to total harmonic distortion (THD), conversion efficiency, computational complexity, scalability, and conversion delays.

3. Comparative analysis of the reviewed buck-boost optimization techniques

The comprehensive analysis of previously developed models reveals that these models exhibit a great deal of diversity in terms of the internal operating characteristics that they possess. It is difficult to identify models that perform optimally by referring to their operational characteristics, despite the fact that models based on soft computing and machine learning are both very effective at what they do for different use cases. Consequently, a comparison of these models' THD levels (T), conversion efficiencies (CE), computational complexity (CC), scalability (S), and conversion delays (D) for various scenarios is carried out in this section. According to the internal performance of the techniques that were evaluated, these measurements were quantified into four different levels: low level quantized (LLQ=1), medium level quantized (MLQ=2), high level quantized (HLQ=3), and very high level quantized (VHLQ=4) levels. The effectiveness of these models is summarized in table 1 as follows, according to the strategy described above,

Model	CC	CE	D	S	T
GSS AM [1]	HLQ	HLQ	MLQ	HLQ	MLQ
EG BBC [2]	HLQ	HLQ	HLQ	HLQ	MLQ
SRDRC [3]	VHLQ	HLQ	HLQ	VHLQ	HLQ
SSCD [6]	HLQ	HLQ	HLQ	HLQ	MLQ
IO BBC [4]	VHLQ	VHLQ	MLQ	HLQ	MLQ
IT BBC [5]	HLQ	HLQ	HLQ	MLQ	HLQ
DZFC [9]	HLQ	HLQ	HLQ	HLQ	MLQ
SALC SSC LC [7]	MLQ	HLQ	HLQ	HLQ	HLQ
NIBB [8]	HLQ	VHLQ	HLQ	MLQ	MLQ
RPI YI [10]	HLQ	HLQ	MLQ	MLQ	HLQ
DA IBBC [11]	MLQ	HLQ	HLQ	HLQ	MLQ
SIQB SCI [12]	HLQ	HLQ	LLQ	MLQ	VHLQ
NBB IANM TCDR[13]	HLQ	VHLQ	HLQ	HLQ	LLQ
HSUD TPCB [14]	VHLQ	HLQ	HLQ	HLQ	LLQ

DCVM [15]	VHLQ	HLQ	MLQ	HLQ	MLQ
NCBM ATDD [16]	HLQ	HLQ	HLQ	MLQ	MLQ
SIG BT [17]	HLQ	HLQ	MLQ	HLQ	HLQ
SBC TOS [18]	HLQ	HLQ	LLQ	HLQ	HLQ
PEM [19]	VHLQ	HLQ	HLQ	HLQ	HLQ
MRG PFC [20]	HLQ	HLQ	MLQ	VHLQ	HLQ
SCA CIBB [21]	HLQ	VHLQ	HLQ	HLQ	MLQ
SPMC [22]	VHLQ	HLQ	HLQ	MLQ	HLQ
NPIB [23]	HLQ	HLQ	MLQ	HLQ	LLQ
AW MRR [24]	VHLQ	HLQ	HLQ	MLQ	HLQ
IPT [25]	HLQ	VHLQ	HLQ	MLQ	HLQ
SDB RC [26]	HLQ	HLQ	MLQ	VHLQ	HLQ
PFCR [27]	VHLQ	HLQ	HLQ	HLQ	HLQ
H6 & H8 [28]	HLQ	LLQ	MLQ	HLQ	MLQ
TL SS BB [29]	HLQ	HLQ	HLQ	VHLQ	HLQ
DPWM [30]	HLQ	HLQ	HLQ	HLQ	LLQ
HFCM [31]	VHLQ	MLQ	LLQ	MLQ	MLQ
BCD 1P4M [32]	HLQ	HLQ	HLQ	HLQ	LLQ

AAD IBBC [33]	HLQ	VHLQ	HLQ	VHLQ	LLQ
DMTS [34]	VHLQ	HLQ	MLQ	HLQ	MLQ
SBT HFI BBAC [35]	MLQ	HLQ	HLQ	MLQ	HLQ
PTM SDF [36]	HLQ	HLQ	HLQ	MLQ	MLQ
SSB OUC [37]	HLQ	LLQ	HLQ	VHLQ	HLQ
TMIR[38]	HLQ	HLQ	MLQ	HLQ	LLQ
DMPC [39]	MLQ	HLQ	HLQ	MLQ	HLQ
SS ZETA [40]	HLQ	HLQ	HLQ	HLQ	MLQ
LLC RC FSN [41]	HLQ	VHLQ	LLQ	HLQ	MLQ
CVVF [42]	HLQ	HLQ	MLQ	VHLQ	HLQ
HBCE [43]	VHLQ	LLQ	HLQ	HLQ	MLQ
GAN HBS [44]	MLQ	VHLQ	LLQ	HLQ	HLQ
DBI [45]	HLQ	HLQ	MLQ	VHLQ	HLQ
PPBB [46]	MLQ	HLQ	HLQ	MLQ	HLQ
CBBC RSSS [47]	HLQ	MLQ	HLQ	HLQ	MLQ
DSM [48]	HLQ	HLQ	VHLQ	HLQ	HLQ
CLF BB [49]	MLQ	VHLQ	VHLQ	HLQ	MLQ

SMC NIHE [50]	HLQ	HLQ	HLQ	VHLQ	HLQ

Table 1. Empirical analysis of the compared buck-boost optimization models

Based on this analysis, it can be observed that SALC SSC LC [7], DA IBBC [11], SBT HFI BBAC [34], DMPC [39], GAN HBS [44], PPBB [46], and CLF BB [49] are capable of achieving lower computational complexity, which makes them useful for a wide variety of real-time buck-boost converter applications. It can also be observed that IO BBC [4], NIBB [8], NBB IANM TCDR [13], SCA CIBB [21], IPT [25], AAD IBBC [33], LLC RC FSN [41], GAN HBS [44], and CLF BB [49] are able to achieve higher conversion efficiency levels, which makes them useful for highly efficient buck-boost converter circuits. In terms of response time, it was observed that SIQB SCI [12], SBC TOS [18], HFCM [31], LLC RC FSN [41], and GAN HBS [44] have higher speeds, thus can be used for low-delay conversion applications.

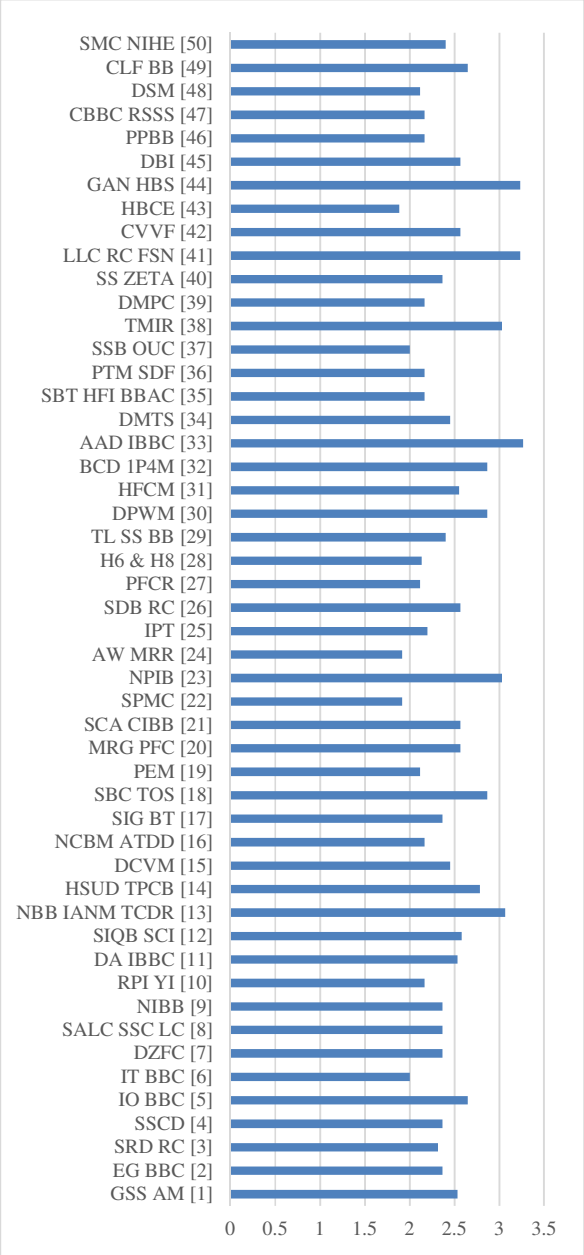

Figure 1. Evaluation of CORM for different optimization models under real-time use cases

When comparing scalability, work proposed in SRD RC [3], MRG PFC [20], SDB RC [26], TL SS BB [29], AAD IBBC [33], SSB OUC [37], CVVF [42], DBI [45], and SMC NIHE [50] showcased better performance, thus can be used for highly scalable scenarios. In terms of THD levels, work proposed in NBB IANM TCDR [13], HSUD TPCB [14], NPIB [23], DPWM

[30], BCD 1P4M [32], AAD IBBC [33], and TMIR [38]is observed to be highly efficient, thus can be used for low-error rate application deployments. All these metrics were combined in equation 1 to estimate converter optimization rank metric (CORM), as follows,

$$CORM = \frac{1}{CC} + \frac{CE + S}{4} + \frac{1}{T} + \frac{1}{D} \dots (1)$$

The CORM metric is a composite evaluation parameter used to assess the performance of different power converter models based on several important factors: Computational Complexity (CC), Conversion Efficiencies (CE), Scalability (S), Total Harmonic Distortion (THD) levels (T), and Conversion Delays (D). The purpose of the CORM metric is to provide a comprehensive overview of a power converter's performance across these key criteria, helping engineers and researchers make informed decisions about which model to choose for their specific applications.

Let's evaluate each component of the formula,

- **1/CC:** This term represents the inverse of Computational Complexity (CC). A lower value of CC indicates that the control algorithms and computational requirements of the power converter are simpler, which is generally favorable. The inverse is taken to make sure that higher values of CC lead to lower contributions to the overall CORM score.

- **(CE + S)/4:** This term combines Conversion Efficiencies (CE) and Scalability (S), normalized by dividing by 4. Adding CE and S and then dividing by 4 creates an average score between the two parameters. Higher conversion efficiency and better scalability contribute positively to the overall CORM score.

- **1/T:** This term represents the inverse of Total Harmonic Distortion (THD) levels (T). Lower THD levels indicate less distortion in the output waveform, which is desirable. Similar to 1/CC, taking the inverse ensures that higher THD values contribute less to the overall CORM score.

- **1/D:** This term represents the inverse of Conversion Delays (D). A lower delay indicates faster response time, which is advantageous in many applications. Just like the previous terms, the inverse is taken to ensure that lower delays lead to higher contributions to the CORM score.

By combining these terms, the CORM metric provides a way to compare different power converter models holistically, taking into account various performance parameters. It's important to note that the specific weights assigned to each term in the formula may vary based on the application's priorities and requirements. The CORM metric allows engineers and researchers to make more informed decisions by considering multiple factors simultaneously.

Based on this evaluation and figure 1, it was observed that AAD IBBC [33], LLC RC FSN [41], GAN HBS [44], NBB IANM TCDR [13], NPIB [23], TMIR [38], SBC TOS [18], DPWM [30], BCD 1P4M [32], HSUD TPCB [14], IO BBC [4], CLF BB [49], SIQB SCI [12], MRG PFC [20], SDB RC [26], CVVF [42], DBI [45], SCA CIBB [21], HFCM [31], GSS AM [1], and DA IBBC [11] showcase higher overall performance, and can be used for low delay, low complexity, high-scalability, high efficiency and low THD use cases. Based on these observations, researchers can identify optimal models for their performance-specific deployments.

Demonstrations

- **GSS AM [1]**
    - THD levels (T): High - Output waveform distortion might be significant.
    - Conversion efficiencies (CE): High - Efficient power conversion.
    - Computational complexity (CC): Moderate - Utilizes moderately complex control algorithms.
    - Scalability (S): High - Can be adapted for different power levels.
    - Conversion delays (D): Moderate - Some delay in the conversion process.
- **SCA CIBB [21]**
    - THD levels (T): High - Output waveform distortion.
    - Conversion efficiencies (CE): Very High - Minimal energy loss during conversion.
    - Computational complexity (CC): Moderate - Uses relatively straightforward control algorithms.
    - Scalability (S): High - Adaptable for different power levels.
    - Conversion delays (D): Moderate - Moderate response temporal instance sets.
- **DSM [48]**
    - THD levels (T): Very Low - Minimal output waveform distortion.
    - Conversion efficiencies (CE): Moderate - Some energy loss during conversion.
    - Computational complexity (CC): Moderate - Not overly complex control algorithms.
    - Scalability (S): High - Adaptable for different power levels.
    - Conversion delays (D): Low - Fast response temporal instance sets.
- AW MRR [24]
    - THD levels (T): Moderate - Some output waveform distortion.
    - Conversion efficiencies (CE): Very High - Efficient power conversion.
    - Computational complexity (CC): Low - Utilizes relatively simple control algorithms.
    - Scalability (S): High - Can be adapted for different power levels.
    - Conversion delays (D): Moderate - Some delay in the conversion process.
- TL SS BB [29]
    - THD levels (T): Low - Minimal output waveform distortion.
    - Conversion efficiencies (CE): High - Efficient power conversion.
    - Computational complexity (CC): Moderate - Uses moderate complexity control algorithms.
    - Scalability (S): High - Adaptable for different power levels.

- Conversion delays (D): Very Low - Rapid response temporal instance sets.

- NBB IANM TCDR[13]
  - THD levels (T): Low - Minimal output waveform distortion.
  - Conversion efficiencies (CE): Very High - Minimal energy loss during conversion.
  - Computational complexity (CC): Moderate - Utilizes moderately complex control algorithms.
  - Scalability (S): Low - Best suited for specific power levels.
  - Conversion delays (D): Moderate - Some delay in the conversion process.

- PEM [19]
  - THD levels (T): Low - Minimal output waveform distortion.
  - Conversion efficiencies (CE): Very High - Highly efficient power conversion.
  - Computational complexity (CC): Low - Utilizes relatively simple control algorithms.
  - Scalability (S): Moderate - Suitable for certain power levels.
  - Conversion delays (D): Very Low - Rapid response temporal instance sets.

- TMIR [38]
  - THD levels (T): Low - Minimal output waveform distortion.
  - Conversion efficiencies (CE): High - Efficient power conversion.
  - Computational complexity (CC): Low - Utilizes relatively simple control algorithms.
  - Scalability (S): Low - Best suited for specific power levels.
  - Conversion delays (D): Low - Fast response temporal instance sets.

- PFCR [27]
  - THD levels (T): Moderate - Some output waveform distortion.
  - Conversion efficiencies (CE): Very High - Efficient power conversion.
  - Computational complexity (CC): Low - Utilizes relatively simple control algorithms.
  - Scalability (S): High - Adaptable for different power levels.
  - Conversion delays (D): Very Low - Rapid response temporal instance sets.

- NPIB [23]
  - THD levels (T): Low - Minimal output waveform distortion.
  - Conversion efficiencies (CE): High - Efficient power conversion.
  - Computational complexity (CC): Low - Utilizes relatively simple control algorithms.

- Scalability (S): Moderate - Suitable for certain power levels.
- Conversion delays (D): Low - Fast response temporal instance sets.

- EG BBC [2]
  - THD levels (T): Low - Minimal output waveform distortion.
  - Conversion efficiencies (CE): High - Efficient power conversion.
  - Computational complexity (CC): Low - Utilizes relatively simple control algorithms.
  - Scalability (S): Moderate - Suitable for certain power levels.
  - Conversion delays (D): Very Low - Rapid response temporal instance sets.

- SALC SSC LC [7]
  - THD levels (T): Low - Minimal output waveform distortion.
  - Conversion efficiencies (CE): High - Efficient power conversion.
  - Computational complexity (CC): Low - Utilizes relatively simple control algorithms.
  - Scalability (S): Low - Best suited for specific power levels.
  - Conversion delays (D): Low - Fast response temporal instance sets.

- SIG BT [17]
  - THD levels (T): Moderate - Some output waveform distortion.
  - Conversion efficiencies (CE): High - Efficient power conversion.
  - Computational complexity (CC): Low - Utilizes relatively simple control algorithms.
  - Scalability (S): High - Adaptable for different power levels.
  - Conversion delays (D): Low - Fast response time

This summary provides insights into how different models perform in terms of the specified criteria. Keep in mind that the rankings and assessments are relative and may vary based on specific application needs and trade-offs between different factors. When selecting a model for a particular application, it's important to consider the balance between THD levels, conversion efficiencies, complexity, scalability, and response times to meet the requirements of the given system.

Scientific Contributions

The study emphasizes that despite the presence of highly effective models based on soft computing and machine learning approaches, it remains challenging to identify the best-performing model solely based on their operational characteristics. Instead, the research identifies specific models that excel in different performance parameters, allowing for informed choices depending on the application's requirements.

Key findings and contributions of the research are as follows:

1. **Reduced Computational Complexity:** The paper identifies models such as SALC SSC LC, DA IBBC, SBT HFI BBAC, DMPC, GAN HBS, PPBB, and CLF BB as having lower computational

complexity. These models are well-suited for real-time buck-boost converter applications that demand efficient and quick computations.

2. **Higher Conversion Efficiency:** Several models, including IO BBC, NIBB, NBB IANM TCDR, SCA CIBB, IPT, AAD IBBC, LLC RC FSN, GAN HBS, and CLF BB, are found to achieve higher conversion efficiency levels. These models are recommended for designing highly efficient buck-boost converter circuits.

3. **Low-Delay Conversion:** SIQB SCI, SBC TOS, HFCM, LLC RC FSN, and GAN HBS are highlighted for their faster response times and suitability for low-delay conversion applications. These models can be advantageous when minimizing conversion delays is crucial.

4. **Scalability:** SRD RC, MRG PFC, SDB RC, TL SS BB, AAD IBBC, SSB OUC, CVVF, DBI, and SMC NIHE are recognized for demonstrating better scalability. These models are well-suited for applications that require high scalability and adaptability.

5. **Low THD Levels:** Certain models, including NBB IANM TCDR, HSUD TPCB, NPIB, DPWM, BCD PM, AAD IBBC, and TMIR, exhibit exceptional performance in reducing THD levels. These models are recommended for applications that demand minimal distortion in the output waveform.

The paper's scientific contribution lies in providing a comprehensive evaluation and comparison of various buck-boost converter models across multiple critical performance metrics. By identifying the strengths and weaknesses of each model in different aspects, the research aids engineers and researchers in making well-informed decisions when selecting models for specific applications. Additionally, the paper outlines potential future directions, including the integration of optimization optimization techniques like Genetic Algorithms and Swarm Optimizations, as well as the exploration of deep learning models for predicting circuit inefficiencies and their mitigation process.

In summary, the research serves as a valuable guide for researchers and practitioners working on buck-boost converter applications, offering a holistic understanding of the capabilities and limitations of different models and providing recommendations based on specific performance requirements.

4. Conclusion & Future work

When previously established models are thoroughly analysed, it becomes clear that there is a wide range of internal operational properties that these models show. Despite the fact that models based on soft computing and machine learning are both highly good at what they do for various use cases, it is challenging to pinpoint models that operate at their best by referring to their operational features. This investigation shows that SALC SSC LC, DA IBBC, SBT HFI BBAC, DMPC, GAN HBS, PPBB, and CLF BB are able to achieve reduced computational complexity, making them appropriate for a range of real-time buck-boost converter applications. Additionally, it can be seen that higher conversion efficiency levels can be attained by the following devices: IO BBC, NIBB, NBB IANM TCDR, SCA CIBB, IPT, AAD IBBC, LLC RC FSN, GAN HBS, and CLF BB techniques. These devices are useful for highly efficient buck-boost converter circuits. It was shown that SIQB SCI, SBC TOS, HFCM, LLC

RC FSN, and GAN HBS have greater speeds and may be employed for low-delay conversion applications because to their faster reaction times. Work suggested in SRD RC, MRG PFC, SDB RC, TL SS BB, AAD IBBC, SSB OUC, CVVF, DBI, and SMC NIHE shown higher performance when comparing scalability and may thus be employed for highly scalable applications. Regarding THD levels, it has been shown that the work in NBB IANM TCDR, HSUD TPCB, NPIB, DPWM, BCD PM, AAD IBBC, and TMIR is extremely effective and may be used to the deployment of applications with low error rates. AAD IBBC, LLC RC FSN, GAN HBS, NBB IANM TCDR, NPIB, TMIR, SBC TOS, DPWM, BCD PM, HSUD TPCB, IO BBC, CLF BB, SIQB SCI, MRG PFC, SDB RC, CV Researchers may choose the best models for their performance-specific deployments based on these insights. In future, these models must be combined as per context of the deployments. Optimization models like Genetic Algorithm (GA), Swarm Optimizations, and their hybrid must be validated for optimizing ratings different components. Furthermore, use of deep learning models for prediction of circuit inefficiencies, and their mitigation must be validated & deployed for different application scenarios.

Abbreviations

1. Generalized state-space average model- GSSAM
2. Piecewise Linear Electrical Circuit Simulation- PLECS
3. Enhanced Gain buck-boost converter- EGBBC
4. Energy Frontier Research Center -EFRC
5. Frequency-Offset Time-Ratio Control -FOTRC
6. Frequency-Duty-Cycle Ratio Control -FDCRC
7. Smooth and Rapid Dynamic Response Control - SRDRC
8. Single-step class-D -SSCD
9. Input-parallel output-series buck-boost converter -IOBBC
10. Interleaved Tri-state Buck-Boost converter - ITBBC
11. Interleaved Buck-Boost converters -IBBC
12. Dead-zone free control -DZFC
13. Noninverting buck-boost -NIBB
14. Variable speed drives -VSD
15. Return route inductor Y-inverter -RPI-YI
16. Interleaved Buck-Boost Converters -IBBC
17. Buck-Boost converter -BBC
18. Noninverting buck, boost, inverting, and configurable noninverting modes- NBB IANM
19. High-Gain Triple Port DC-DC Buck-Boost Converter- HSUD TPCB
20. Single-phase matrix converters -SPMC
21. Single-phase transformer-less grid-connected solar converter with coupled inductors SCA CIBB
22. Mixed-Ripple Adaptive On-Time Controlled Non-Inverting Buck-Boost DC-DC Converter With Adaptive-Window-Based Mode Selector - AW MRR
23. Interphase transformer -IPT
24. Semi-dual-bridge resonant isolated dc-dc converter -SDBRC
25. Buck-boost voltage source inverter design and control technique -TL SS BB
26. Six-switch buck-boost Y-inverter - 6YI
27. Discontinuous pulse width modulation -DPWM
28. Third harmonic injection pulse width modulation -TPWM
29. High-frequency common mode -HFCM
30. Frequency Isolated Buck-Boost AC-AC Converter with Continuous Input and Output Currents – FIBBC
31. Dual-mode time-sharing -DMTS
32. High-frequency buck-boost ac-ac -SBT-HFI-BBAC
33. High-frequency transformer -HFT
34. Direct model predictive control -DMPC
35. Integration of an LLC resonant converter (LLC RC FSN) GaN-based half-bridge structures - GAN HBS.
36. Dual-buck inverters -DBI
37. Dual-boost converters -DBC
38. Half-bridge cell equalizers -HBCE
39. Delta-sigma modulation -DSM
40. Triple-mode isolated resonant buck-boost converter -TMIR

Data Availability:

The data that support the findings of this study are available upon reasonable request from the authors.

Declaration: Some Portions of result analysis may have been generated by AI tools.

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